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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/811,456	03/20/2001	Masahito Isoda	108075-00056	2125

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EXAMINER
NGUYEN, LONG T

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 05/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/811,456	ISODA, MASAHITO	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *22-37* is/are allowed.

6)☒ Claim(s) *19 and 38* is/are rejected.

7)☒ Claim(s) *20,21 and 39-42* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *19 March 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/479,927* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. This office action is responsive to the amendment filed on 3/19/02.

2. The objection to the drawings and the rejection under 35 U.S.C. 112, 2nd paragraph in the last office action (mailed on 10/19/01) has been overcome base on applicant's amendment.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 19 and 38 are rejected under 35 U.S.C. 102(b) as being anticipated by Park (USP 5,920,208).

With respect to claim 19, Figure 1 of the Park reference disclose a circuit which includes: a differential amplifier circuit (20-24, 30), disposed between a first power supply (Vcc) and a second power supply (Vss) for receiving first and second input signals (D, DB) and generating an amplifier signal (node N2) corresponding to a voltage difference between the first and second input signals; a first circuit (31-36) for receiving the amplified signal (node N2 connected to gate of 35) from the differential amplifier circuit; a second circuit (25-30), disposed between the first power supply Vcc and second power supply Vss, for receiving the first input signal (D); and a control circuit (1), for selectively enabling the differential amplifier circuit and the second circuit in accordance with a control signal (ATD), wherein the control circuit isolates one of the differential amplifier circuit and the second circuit from at least one of the first power supply and

the second power supply (when the output of control circuit 1 disables transistor 30, the amplifier and the second circuit are isolated from the second power supply Vss). Note that, for broad reasonable interpretation, it only needed at least one circuit to isolate from only one power supply to meet the limitation "wherein the control circuit isolates one of the differential amplifier circuit and the second circuit from at least one of the first power supply and the second power supply", e.g. it only needs either one of the differential amplifier or the second circuit to isolate from either one of the first power or the second power.

With respect to claim 38, Figure 1 of the Park reference disclose a circuit which includes: a differential amplifier circuit (20-24, 30), disposed between a first power supply (Vcc) and a second power supply (Vss) for receiving first and second input signals (D, DB) and generating an amplifier signal (node N2) corresponding to a voltage difference between the first and second input signals; a first circuit (31-36), disposed between the first power supply (Vcc) and the second power supply (Vss), for receiving the amplified signal (node N2 connected to gate of 35) from the differential amplifier circuit; a second circuit (25-30), disposed between the first power supply Vcc and second power supply Vss, for receiving the first input signal (D); and a control circuit (1), connected to the differential amplifier circuit and the first and second circuits, for selectively enabling the first circuit and the second circuit in accordance with a control signal (ATD), wherein the control circuit isolates one of the first circuit and the second circuit from at least one of the first power supply and the second power supply (when the output of control circuit 1 disables transistor 30 and transistor 36, the first circuit and the second circuit are isolated from the second power supply Vss).

5. Claim 19 is also rejected under 35 U.S.C. 102(b) as being anticipated by Roe et al. (USP 5,929,655).

With respect to claim 19, Figure 3 of the Roe et al. reference disclose an input buffer circuit which includes: a differential amplifier circuit (210), disposed between a first power supply (Vdd) and a second power supply (Gnd) which can be seen in Figure 4 (amplifier 210 in Figure 3 is the combination of transistors 322, 324, 326, 328, 330, 332, 334 and 336 in Figure 4) for receiving first and second input signals (140, 146) and generating an amplifier signal (output of 210) corresponding to a voltage difference between the first and second input signals; a first circuit (208) for receiving the amplified signal from the differential amplifier circuit; a second circuit (202), inherently disposed between the first power supply Vdd and second power supply Gnd, for receiving the first input signal (140); and a control circuit (214) for selectively enabling the differential amplifier circuit and the second circuit in accordance with a control signal (DIFF_EN, OUTA_EN, OUTB_EN), wherein the control circuit isolates one of the differential amplifier circuit and the second circuit from at least one of the first power supply and the second power supply (the differential amplifier 213 in Figure 3 is shown in detail as the combination of transistors 322, 324, 326, 328, 330, 332, 334 and 336 in Figure 4, and when the control circuit disables transistor 322, the amplifier is isolated from the second power supply Gnd).

Response to Arguments

6. Applicant's arguments filed on 3/19/02 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

7. Claims 20, 21 and 39-42 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 20 would be allowed because none of the prior art of record discloses or suggests an input buffer circuit which includes all the limitations of this claim. In particular, applicant's arguments are found persuasive that the prior art of record fails to disclose or suggest, in combination with other limitations, the "control circuit enables the differential amplifier circuit and disables the second circuit when the first and second input signals have amplitudes smaller than a predetermined voltage".

Claim 21 would be allowed because none of the prior art of record discloses or suggests an input buffer circuit which includes all the limitations of this claim. In particular, applicant's arguments are found persuasive that the prior art of record fails to disclose or suggest, in combination with other limitations, the "control circuit disables the differential amplifier circuit and enables the second circuit when the first and second input signals have amplitudes greater than a predetermined voltage".

Claim 39 would be allowed because none of the prior art of record discloses or suggests an input buffer circuit which includes all the limitations of this claim. In particular, applicant's arguments are found persuasive that the prior art of record fails to disclose or suggest, in combination with other limitations, the "control circuit isolates the first circuit from the first power supply or the second power supply when the first and second input signals have amplitudes smaller than a predetermined voltage".

Claim 40 would be allowed because none of the prior art of record discloses or suggests an input buffer circuit which includes all the limitations of this claim. In particular, applicant's arguments are found persuasive that the prior art of record fails to disclose or suggest, in combination with other limitations, the "control circuit isolates the second circuit from the first power supply or the second power supply when the first and second input signals have amplitudes greater than a predetermined voltage".

Claim 41 would be allowed because none of the prior art of record discloses or suggests an input buffer circuit which includes all the limitations of this claim. In particular, applicant's arguments are found persuasive that the prior art of record fails to disclose or suggest, in combination with other limitations, the "control circuit enables the differential amplifier circuit and the first circuit and disables the second circuit when the first and second input signals have amplitudes smaller than a predetermined voltage".

Claim 42 would be allowed because none of the prior art of record discloses or suggests an input buffer circuit which includes all the limitations of this claim. In particular, applicant's arguments are found persuasive that the prior art of record fails to disclose or suggest, in combination with other limitations, the "control circuit disables the differential amplifier circuit and the first circuit and enables the second circuit when the first and second input signals have amplitudes greater than a predetermined voltage".

8. Claims 22-37 are allowed.

Claims 22 and 28 are allowed because none of the prior art of record discloses or suggests an input buffer circuit which includes all the limitations of this claim. In particular, applicant's arguments are found persuasive that the prior art of record fails to disclose or suggest,

in combination with other limitations, the "control circuit enables the differential amplifier circuit and disables the second circuit when the first and second input signals have amplitudes smaller than a predetermined voltage".

Claims 23-24 and 29-32 are allowed because they depend on claims 22 and 28, respectively.

Claims 25 and 33 are allowed because none of the prior art of record discloses or suggests an input buffer circuit which includes all the limitations of this claim. In particular, applicant's arguments are found persuasive that the prior art of record fails to disclose or suggest, in combination with other limitations, the "control circuit disables the differential amplifier circuit and enables the second circuit when the first and second input signals have amplitudes greater than a predetermined voltage".

Claims 26-27 and 34-37 are allowed because they depend on claims 25 and 33, respectively.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Long Nguyen whose telephone number is (703) 308-6063. The examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax number for this group is (703) 308-7722.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is (703) 308-0956.

April 27, 2002

L N

Long Nguyen
Art Unit: 2816

Terry D. Cunningham
Primary Examiner